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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Doris, et al.

Serial No.:	10/710,272	**Group Art Unit**:	2812
Filed:	June 30, 2004	**Examiner**:	Tsai, H.
For:	METHOD AND STRUCTURE FOR STRAINED FINFET DEVICES		

Commissioner of Patents
Alexanderia, VA 22313-1450

APPELLANTS' BRIEF ON APPEAL (as revised 4/19/07)

Sir:

Appellants respectfully appeal the rejection of claims 1-15 and 23-30 in the Office Action dated September 11, 2006. A Notice of Appeal was timely filed on December 11, 2006.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-15 and 23-30 are all the claims presently pending in the application. Claims 16-22 are withdrawn as being directed toward a non-elected invention and are not the object of this Appeal. Claims 1-15, and 23-30 stand rejected under 35 U.S.C. § 102(e) as anticipated by US Patent 6,909,151 to Hareland.

The rejection for claims 1-15 and 23-30 are being appealed.

IV. STATUS OF AMENDMENTS

A Request for Reconsideration Under 37 CFR §1.116 was filed on November 13, 2006. Therefore, the version of the claims in the Appendix reflects the claim amendments of the Amendment Under 37 CFR §1.111 filed on December 7, 2005.

In the Advisory Action mailed December 6, 2006, the Examiner indicated that the arguments in the Amendment Under 37 CFR §1.116 were not persuasive and that the rejection based on Hareland was maintained.

It is noted the Examiner's comments in the Advisory Action is the first time during prosecution that the Examiner seems to reasonably attempt to address Appellants' requests that the Examiner explain how this reference is being interpreted, since Hareland shows a layer 360 that is clearly global to the device, rather than being localized within the device. Therefore, Appellants will be addressing, as appropriate, some of the points raised in the Advisory Action as part of this Appeal Brief.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Appellants' invention, as disclosed and as claimed in independent claim 1, is directed to a method of forming an electronic device, said method including forming at least one localized stressor region within the device.

As explained at lines 14-15 of page 4 of the disclosure, strained silicon is conventionally grown epitaxially as a layer on a SiGe layer structure, but, as explained at lines 8-10 of page 6, such strained silicon has been difficult to integrate in FinFET devices because of the geometry of the fin and gate and because of the fabrication process.

Therefore, Appellants have developed the concept of the present invention, wherein stressor regions are formed locally within the device. In the exemplary embodiment discussed in the disclosure, a FinFET device is used to demonstrate the process of incorporating a stressor region on specific components within the FinFET structure.

The locations within the specification and figures of the claimed invention for the independent claims are as follows:

Independent Claim 1. A method of forming an electronic device 600, 700 (see Figs. 6 & 7), said method comprising:

forming at least one localized stressor region (areas 601, 701) within said device 600, 700 [para 0027, 0033, 0035, 0036].

Independent Claim 14. A method of forming a stress region in an electronic device, said method comprising:

forming a first localized stressor region 601 (left side) within said device 600; and

forming a second localized stressor region 601 (right side) within said device 600,

said first localized stressor region and said second localized stressor region causing a region therebetween to be stressed (Fig. 10) [para. 0027, 0033, 0035, 0036].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellants present the following issue for review by the Board of Patent Appeals and Interferences:

ISSUE #1: THE 35 U.S.C. § 102(e) REJECTION FOR CLAIMS 1-15 AND 23-30 BASED ON U.S. PATENT 6,909,151 TO HARELAND ET AL.

Whether the rejection under 35 U.S.C. § 102(e) can be maintained for any of the rejected claims 1-15 and 23-30.

VII. ARGUMENTS

ISSUE #1: THE REJECTION AS BASED ON HARELAND

Appellants believe that it is clear that the stressor layer 360,560 of Hareland is clearly applied globally to the device 300, not locally within the device, as required by the plain meaning of the claim language of the independent claims, and that Hareland fails to describe any other stressor region, let alone a localized stressor region.

A. THE EXAMINER'S POSITION ON THE REJECTIONS BASED ON HARELAND

The Examiner alleges that claims 1-15 and 23-30 are anticipated by Hareland. From Appellants' perspective, as best understood, based on the Examiner's comments in the Advisory Action mailed on December 6, 2006, the most relevant part of the final rejection is the following paragraph on page 2 of the Office Action mailed on September 11, 2006, and substantially repeated in the conclusion on page 4:

> "*... forming at least one localized stressor region (stress incorporating layer formed above of (sic) beneath the channel region, such as silicon nitride layer 360 or 560 or oxide layer 319 or Cobalt silicide 430, same material as instant invention) within the device, col. 2, lines 33-67, col. 6, line 28-67, figs. 3-4....*"

Based on the comments in the attachment page 2 of the Advisory Action, containing the continuation of 11, the Examiner is understood as alleging that, because there is a silicon nitride layer, an oxide layer, or cobalt silicide used in Hareland, then such components inherently provide a stressor region.

Thus, as best understood, the Examiner is alleging that Hareland actually provides a number of stressor regions, even though the reference itself describes only layer 360,560 as being a stressor region. Moreover, the Examiner is understood as alleging that, by characterizing Hareland as having more stressor regions than actually described in the reference itself, the initial burden of a *prima facie* rejection has been met and the Examiner considers that the burden has been shifted back to Appellants.

Finally, based on the clarification in the Advisory Action, the Examiner further considers that Appellants failed to properly address the Examiner's presumption and characterization concerning the additional stressor regions, so that the rejection is maintained.

B. APPELLANTS' POSITION ON THE REJECTION BASED ON HARELAND

Appellants submit that the Examiner's position above errs both as a matter of law and as a matter of fact.

Appellants first submit that the rationale in the above-recited passage from the final rejection, as clarified by comments in the Advisory Action, is error as a matter of law. The Examiner is seemingly attempting to allege that any use of silicon nitride, oxide, or cobalt silicide near a channel region constitutes a stressor region relative to that channel.

As such, the Examiner is proposing an inherency argument, and Appellants submit that the Examiner's initial burden is not met unless such inherency is demonstrated on the record.

Moreover, the cited prior art reference Hareland itself only describes the silicon nitride layer 360,560 as a stressor. No other layer or component in Hareland is described as constituting a stressor region, let alone a localized stressor region.

Appellants, therefore, respectfully submit that the rejection currently of record fails to meet the initial burden of a *prima facie* rejection, since the prior art reference does not provide a description of a localized stressor region and because the rejection currently of record fails to demonstrate the inherency that would be required to support the Examiner's position.

Second, as a matter of fact, neither the present disclosure nor Hareland describes that any use of silicon nitride, oxide, or cobalt silicide near a channel region creates a stressor region.

That is, Hareland clearly describes only the film 360,560 as creating the stressor region, and these films are clearly global over the device, not localized, as required to

satisfy the plain meaning of the claim language. Hareland does not describe any of the other structures (e.g., oxide layer 319 or cobalt silicide 430) as providing a stressor region.

Moreover, in column 13 Hareland clearly describes that the silicon nitride film can be used as a stressor if the silicon nitride film is compressive (line 23, for NMOS) or tensile (line 36, for PMOS).

This description of silicon nitride as having to be specifically formed to be either compressive or tensile is different from alleging that silicon nitride is inherently either compressive or tensile. This description of silicon nitride as specifically formed to be either compressive SiN or tensile SiN is supported by the description in paragraphs [0033] ("*One choice for the compressive material is compressive SiN.*") and [0035] ("*One choice for the tensile material is tensile SiN.*") of the present disclosure.

However, nowhere does either Hareland or the present disclosure suggest that SiN is inherently compressive/tensile. Indeed, both references clearly indicate that SiN can be either compressive or tensile, and Appellants submit that it should be apparent that a SiN may be neither compressive nor tensile.

That is, as explained, for example in line 66 of column 8 through line 18 of column 9 of US Patent 6,960,781 to Currie et al., the characteristic of whether silicon nitride is compressive or tensile is not inherent to generic silicon nitride, but rather by its formation and exact composition, explained in Currie, as follows:

"*The strain of silicon nitride films grown by LPCVD at temperatures greater than approximately 700^0 C. may be selected by varying the silicon content of the nitride film. (See, e.g., S. Habermehl,* J. Appl. Phys., *83(9) p. 4672 (1998), incorporated herein by reference.) For example, LPCVD stoichiometric silicon nitride films (i.e., Si_3N_4) are typically tensilely strained, while silicon-rich nitride films (e.g., with a silicon volume fraction greater than 0.1-0.15, or with a Si/N atomic ratio greater than 0.75) are typically compressively strained. The silicon content of a nitride film formed by LPCVD may be varied by changes in the ratio of silicon and nitrogen precursors utilized in the growth process. For example, a nitride growth process performed at 850^0 C. and a pressure of 200 milliTorr (mTorr) utilizing dichlorosilane ($SiCl_2H_2$) as a silicon precursor and ammonia (NH_3) as a nitrogen precursor will form a silicon–rich nitride when the ratio of*

dichlorosilane flow to the total gas flow is greater than approximately 0.85. For lower temperatures, the relative amount of dichlorosilane may need to be increased to form silicon-rich nitride films."

Thus, Appellants submit that, since Hareland clearly describes the silicon nitride layer 360, 560 as either compressive or tensile, the Examiner can reasonably rely upon this description for this layer as being a compressive/ tensile stressor region, albeit, globally applied to the device. There is no suggestion in Hareland to apply silicon nitride as a localized stressor region.

Relative to the Examiner's characterization that the present disclosure provides a teaching similar to using "oxide layer 319 or Cobalt silicide 430", Appellants can find no reference in the present disclosure relative to an "oxide layer" as providing the localized stressor. Therefore, Appellants make no further comment concerning oxide layers in the cited prior art, except to note that the Examiner fails to point to any specific line in Hareland that describes an oxide layer as either compressive/tensile, get alone a localized stressor region.

It appears the Examiner's position relative to cobalt silicide is derived from the final sentence in paragraph [0033] ("*Another choice is to silicide the open hole, without etching the Si region, using a highly compressive silicide, such as PdSi, Pt silicide, or the like.*"), but, more likely, from the final paragraph in paragraph [0035] ("*Another choice is to silicide the open hole, without etching the Si region, using a highly tensile silicide like, for example, $CoSi_2$ silicide.*").

However, neither of these two final sentences are describing that "cobalt silicide" inherently generates a stressor, as the rejection currently of record presumes, and Appellants submit that the strain quality of the silicide depends upon whether the silicide is rich in silicon, similar to the description above from Currie, relative to causing silicon nitride to be either compressive or tensile. There is no description in the present Application that any "cobalt silicide" will be a stressor region, and there does not appear to be a description in Hareland that a specific cobalt silicide has been implemented to be a stressor region.

Therefore, Appellants again respectfully submit that the rejection currently of record has failed to provide a *prima facie* rejection for anticipation of even the independent claims.

CONCLUSION

In view of the foregoing, Appellants submit that claims 1-15 and 23-30, all the claims presently rejected in the application, are clearly enabled and patentably distinct from the prior art of record and in condition for allowance. Thus, the Board is respectfully requested to remove the rejection of claims 1-15 and 23-30 based on Hareland.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Assignee's Deposit Account number 09-0458.

Respectfully submitted,

Dated: 4/18/07 (as revised per Not'n of Non-Compliant Appeal Brief mailed 4/13/07)

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VIII. CLAIMS APPENDIX

Claims, as reflected upon entry of the Amendment Under 37 CFR §1.116 filed on December 7, 2005:

1. (Rejected) A method of forming an electronic device, said method comprising:

forming at least one localized stressor region within said device.

2. (Rejected) The method of claim 1, wherein said at least one localized stressor region comprises a first localized stressor region, said method further comprising:

forming a second localized stressor region within said device,

said first localized stressor region and said second localized stressor region causing a region therebetween to be stressed.

3. (Rejected) The method of claim 2, wherein said first localized stressor region and said second localized stressor region comprise a same type material.

4. (Rejected) The method of claim 3, wherein said same type material comprises one of a compressive stressor material and a tensile stressor material.

5. (Rejected) The method of claim 2, wherein said device comprises a FinFET (Fin Field Effect Transistor).

6. (Rejected) The method of claim 5, wherein said FinFET contains a plurality of fins interconnected by fin connectors and said first and second localized stressor regions are formed on said fin connectors of said FinFET.

7. (Rejected) The method of claim 5, wherein said first and second localized stressor regions are formed on a source and drain region of said FinFET.

8. (Rejected) The method of claim 2, wherein said device comprises a planar FET (Field Effect Transistor).

9. (Rejected) The method of claim 8, wherein said stressor regions are formed on a source and drain region of said planar FET.

10. (Rejected) The method of claim 4, wherein said same type material comprises a compressive material and primary charge carriers in said region being stressed comprise holes.

11. (Rejected) The method of claim 4, wherein said same type material comprises a tensile material and primary charge carriers in said region being stressed comprise electrons.

12. (Rejected) The method of claim 2, wherein said region being stressed causes a carrier mobility in said stressed region to be one of increased and decreased, relative to a carrier mobility in a region without said stress.

13. (Rejected) The method of claim 1, wherein said device comprises one of a plurality of devices in an electronic circuit, said method further comprising:

selectively providing a blocking mask over devices in said electronic circuit which are not to receive said at least one localized stressor region.

14. (Rejected) A method of forming a stress region in an electronic device, said method comprising:

forming a first localized stressor region within said device; and

forming a second localized stressor region within said device,

said first localized stressor region and said second localized stressor region causing a region therebetween to be stressed.

15. (Rejected) The method of claim 14, wherein said region being stressed causes a carrier mobility in said stressed region to be one of increased and decreased, relative to a carrier mobility in a region without said stress.

16-22. (Withdrawn)

23. (Rejected) The method of claim 1, wherein at least one of said at least one localized stressor region interacts with a stressed region located outside said device.

24. (Rejected) The method of claim 1, wherein said at least one localized stressor region is used to generate one of a compression stress and a tensile stress.

25. (Rejected) The method of claim 1, wherein said at least one localized stressor region is located within said device to generate a stress that enhances a performance of said device.

26. (Rejected) The method of claim 25, wherein said performance enhancement comprises an increase in a carrier mobility.

27. (Rejected) The method of claim 25, wherein said performance enhancement comprises a decrease in a carrier mobility.

28. (Rejected) The method of claim 1, wherein said at least one localized stressor region is located to generate a stressed region in at least one of a direction parallel to a current flow and perpendicular to a current flow.

29. (Rejected) The method of claim 1, wherein said at least one localized stressor region is used to create a symmetrically stressed region.

30. (Rejected) The method of claim 1, wherein said at least one localized stressor region is used to create an asymmetrically stressed region.

IX. EVIDENCE APPENDIX

(NONE)

X. RELATED PROCEEDINGS APPENDIX

(NONE)